MAGMIO

Testing FPGA in Software with Magmio

We understand that starting with FPGA is a big commitment and a difficult decision. Therefore, we offer you to test the behavior and performance of the FPGA technology entirely in software before buying the actual hardware.

Magmio Model

Magmio Model implements a complete FPGA processing pipeline in C++ and uses the same API as the physical hardware.

It's possible to compile your strategy in C or C++ against the Model and use it to test the trading strategy with PCAP data or even with real exchange access.

Since Magmio Model is a software-based application, it is ideal for rapid testing, prototyping, and getting familiar with our product without purchasing the FPGA card.

The Model is also valuable later on in production for testing new strategies and ideas in software before deploying to the production environment on the FPGA. These rapid software iterations save both time and money.

HLS Compiler

The other part is the Vivado HLS compiler. It provides the translation of C or C++ code into Hardware Description Language (VHDL or Verilog).

Since FPGA design is entirely deterministic, the compiler can report the exact latency and resource consumption without running the strategy in an actual FPGA chip.

This evaluation verifies the performance and feasibility of your algorithm in the FPGA hardware without paying the full cost of the license. We make sure that FPGA technology is the right path for you to move forward.

If you find the results satisfying, we will provide a smooth transition of your trading strategy into the Magmio platform. Our time-to-market is usually only a few weeks.

For more information do not hesitate to contact us:

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